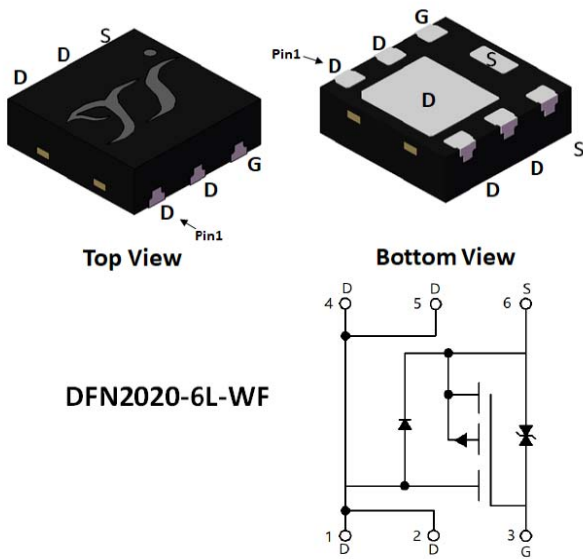


P-Channel Enhancement Mode Field Effect Transistor



Product Summary

- V_{DS} -20V
- I_D -8.4A
- $R_{DS(ON)}$ (at $V_{GS}=-4.5V$) < 80m Ω
- $R_{DS(ON)}$ (at $V_{GS}=-2.5V$) < 154m Ω
- ESD Protected Up to 2.0KV (HBM)

General Description

- High Power and Current handling capability
- Low Gate Charge
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free
- Part no. with suffix "Q" means AEC-Q101 qualified

Applications

- PWM applications
- Power management
- Load switch

Limiting Values

Parameter	Conditions		Symbol	Min	Max	Unit		
Drain-source Voltage			V_{DS}	-	-20	V		
Gate-source Voltage			V_{GS}	-12	12			
Continuous Drain Current (Note 1,2)	Steady-State	$T_A=25^\circ C, V_{GS}=-4.5V$	I_D	-	-3.4	A		
		$T_A=100^\circ C, V_{GS}=-4.5V$		-	-2.1			
Continuous Drain Current (Note 1,3)	Steady-State	$T_C=25^\circ C, V_{GS}=-4.5V$, Chip limitation		-	-8.4			
		$T_C=100^\circ C, V_{GS}=-4.5V$		-	-5.3			
Pulsed Drain Current	$T_C=25^\circ C, t_p \leq 10\mu s$		I_{DM}	-	-33.6			
Maximum Body-Diode Continuous Current	$T_C=25^\circ C$		I_S		-6.9			
Total Power Dissipation (Note 1,2)	Steady-State	$T_A=25^\circ C$	P_D	-	1.38	W		
		$T_A=100^\circ C$		-	0.55			
Total Power Dissipation (Note 1,3)	Steady-State	$T_C=25^\circ C$		-	8.3			
		$T_C=100^\circ C$		-	3.3			
Junction and Storage Temperature Range				T_J, T_{STG}	-55		150	$^\circ C$

Thermal Resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient (Note 2)	Steady-State	$R_{\theta JA}$	-	90	$^\circ C/W$
Thermal Resistance Junction-to-Case	Steady-State	$R_{\theta JC}$	-	15	



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■ Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=-250\mu A, T_j=25^\circ C$	-20	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=-20V, V_{GS}=0V, T_j=25^\circ C$	-	-	-1	μA
		$V_{DS}=-20V, V_{GS}=0V, T_j=150^\circ C$	-	-	-100	
Gate-Source Leakage Current	I_{GSS}	$V_{GS}=\pm 12V, V_{DS}=0V, T_j=25^\circ C$	-	-	± 10	
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A, T_j=25^\circ C$	-0.5	-1	-1.5	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=-4.5V, I_D=-4A, T_j=25^\circ C$	-	61	80	$m\Omega$
		$V_{GS}=-2.5V, I_D=-2A, T_j=25^\circ C$	-	103	154	$m\Omega$
Diode Forward Voltage	V_{SD}	$I_S=-4A, V_{GS}=0V, T_j=25^\circ C$	-	-0.94	-1.2	V
Gate Resistance	R_G	$f=1MHz, T_j=25^\circ C$	-	15	-	Ω
Dynamic Parameters						
Input Capacitance	C_{iss}	$V_{DS}=-10V, V_{GS}=0V, f=1MHz, T_j=25^\circ C$	-	445	668	pF
Output Capacitance	C_{oss}		-	103	-	
Reverse Transfer Capacitance	C_{rss}		-	72	-	
Switching Parameters						
Total Gate Charge	Q_g	$V_{GS}=-4.5V, V_{DS}=-10V, I_D=-4A, T_j=25^\circ C$	-	5.2	-	nC
Gate-Source Charge	Q_{gs}		-	1.3	-	
Gate-Drain Charge	Q_{gd}		-	1.1	-	
Reverse Recovery Charge	Q_{rr}	$I_F=-4A, di/dt=100A/\mu s, V_{GS}=0V, V_R=-10V, T_j=25^\circ C$	-	14.3	-	nC
Reverse Recovery Time	t_{rr}		-	20.4	-	ns
Turn-on Delay Time	$t_{D(on)}$	$V_{GS}=-4.5V, V_{DS}=-10V, I_D=-4A, R_{GEN}=3\Omega, T_j=25^\circ C$	-	9.4	-	ns
Turn-on Rise Time	t_r		-	19.5	-	
Turn-off Delay Time	$t_{D(off)}$		-	23	-	
Turn-off Fall Time	t_f		-	13.2	-	

Note:

- The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
- The value of $R_{\theta JA}$ is measured with the device mounted on the 40mm*40mm*1.1mm single layer FR-4 PCB board with 1 in² pad of 2oz. Copper, in the still air environment with $T_A=25^\circ C$. The maximum allowed junction temperature of 150 $^\circ C$. The value in any given application depends on the user's specific board design.
- Thermal resistance from junction to soldering point (on the exposed drain pad).



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Typical Electrical and Thermal Characteristics Diagrams

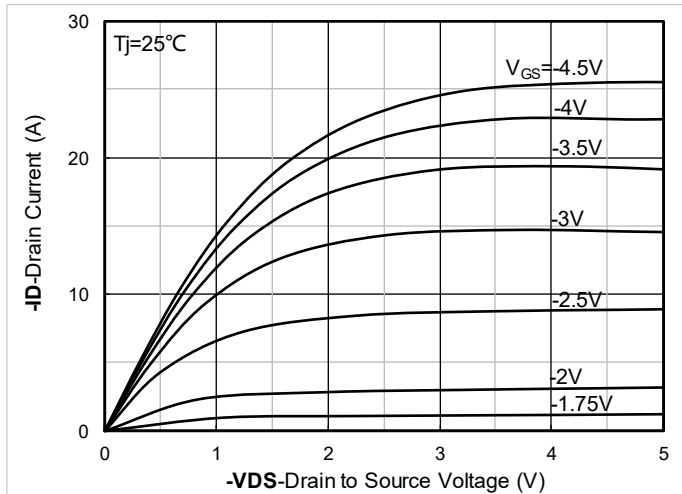


Figure 1. Output Characteristics; typical values

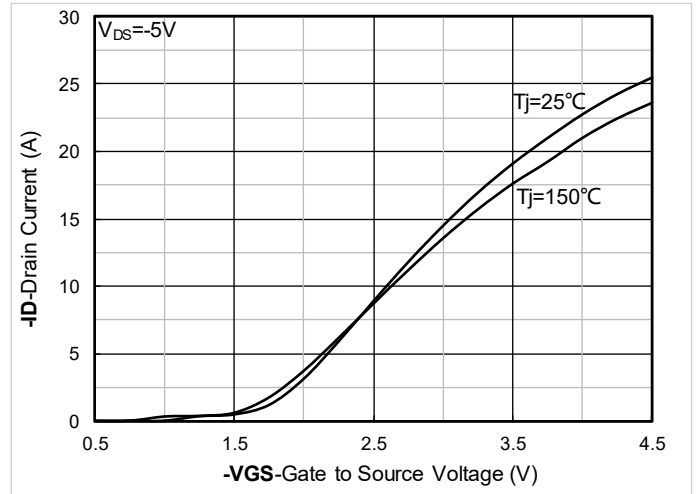


Figure 2. Transfer Characteristics; typical values

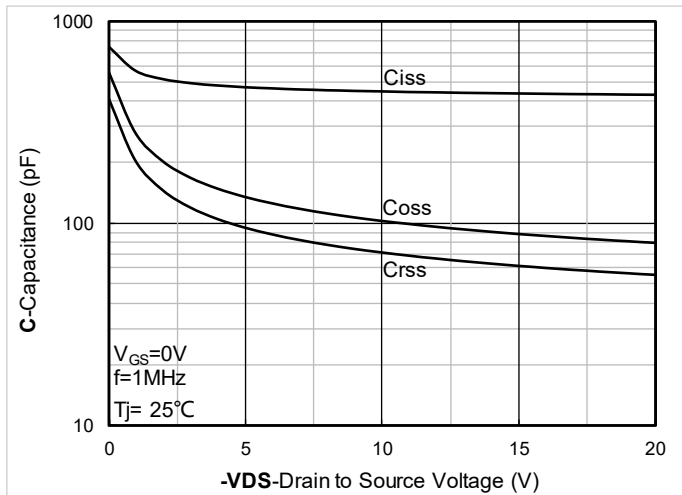


Figure 3. Capacitance Characteristics; typical values

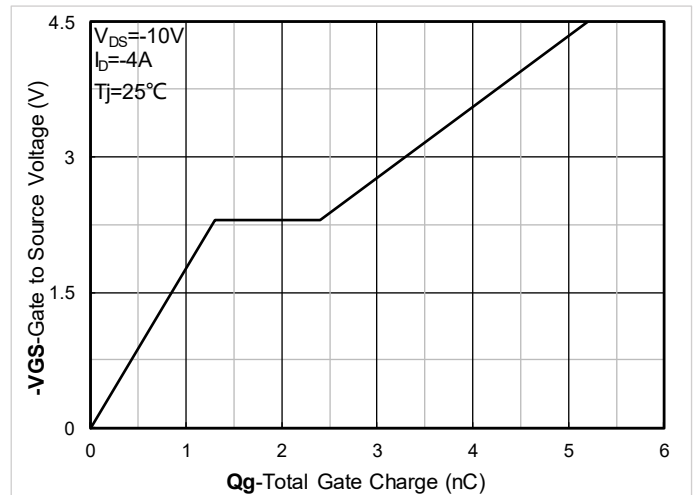


Figure 4. Gate Charge; typical values

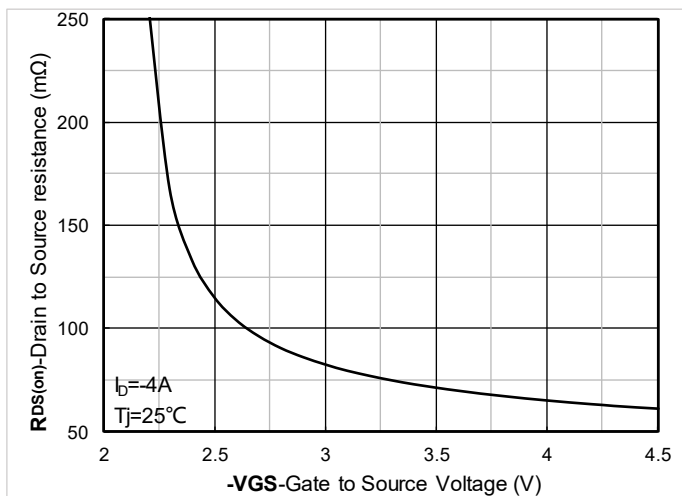


Figure 5. On-Resistance vs Gate to Source Voltage; typical values

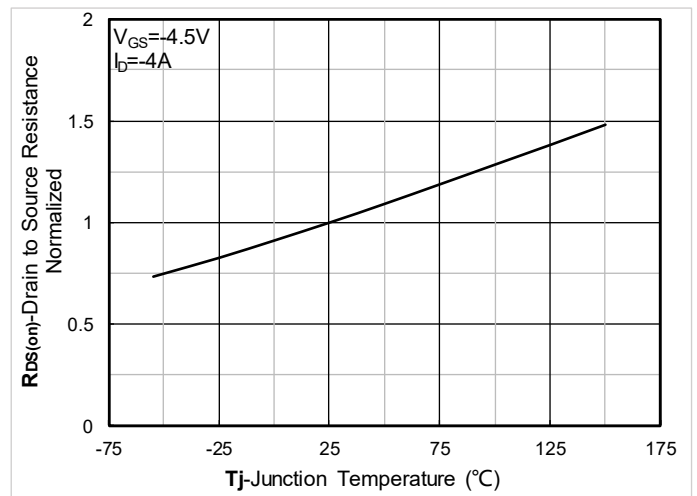


Figure 6. Normalized On-Resistance



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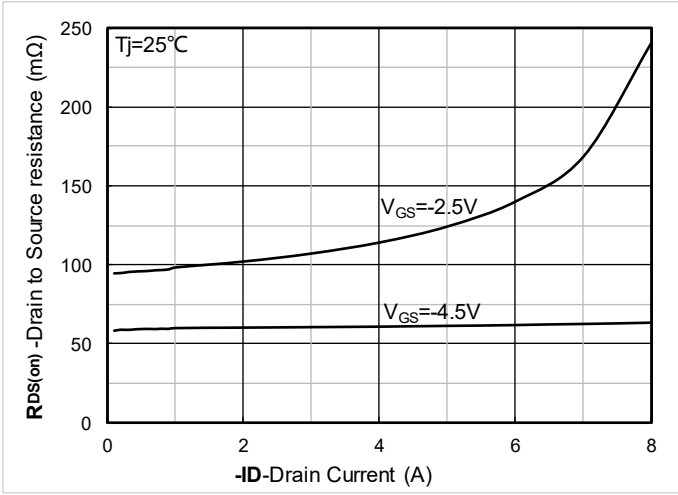


Figure 7. RDS(on) VS Drain Current; typical values

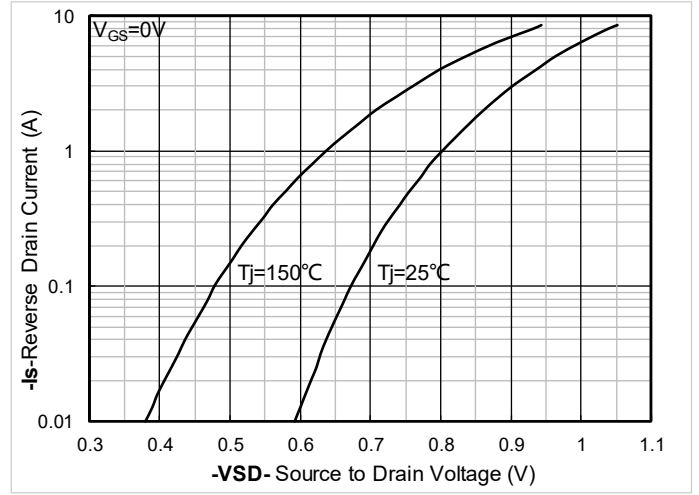


Figure 8. Forward characteristics of reverse diode; typical values

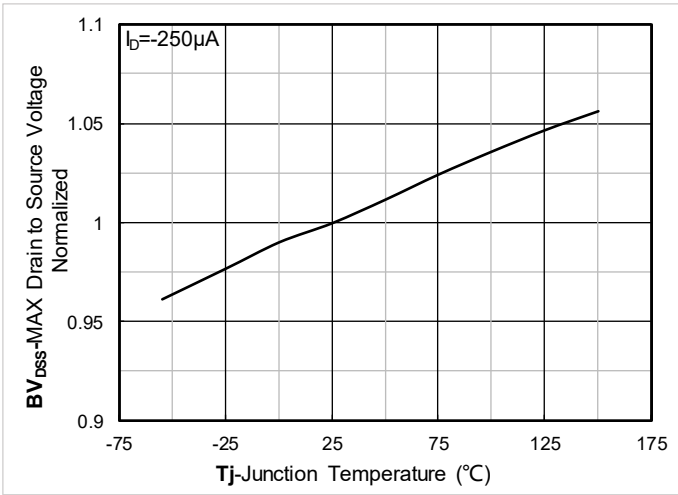


Figure 9. Normalized breakdown voltage

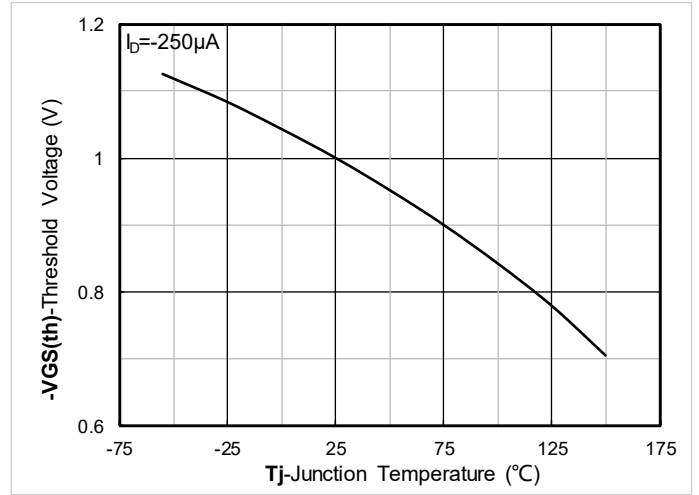


Figure 10. Gate Threshold voltage; typical values

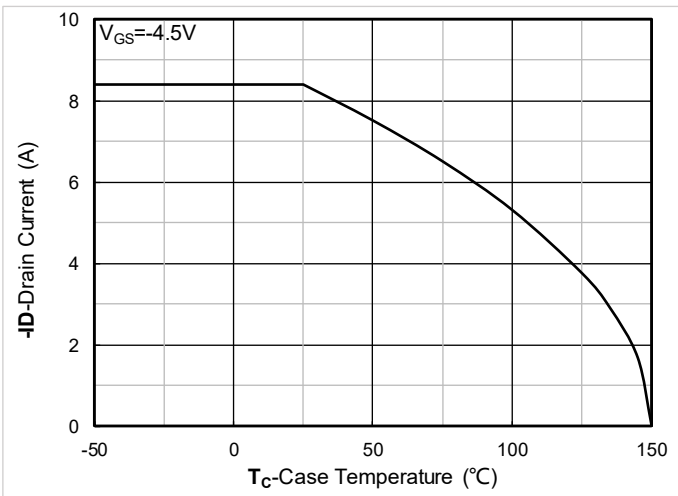


Figure 11. Current dissipation

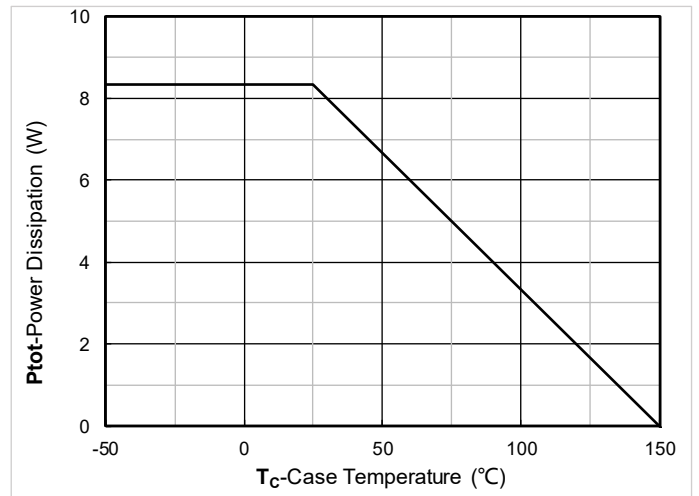


Figure 12. Power dissipation



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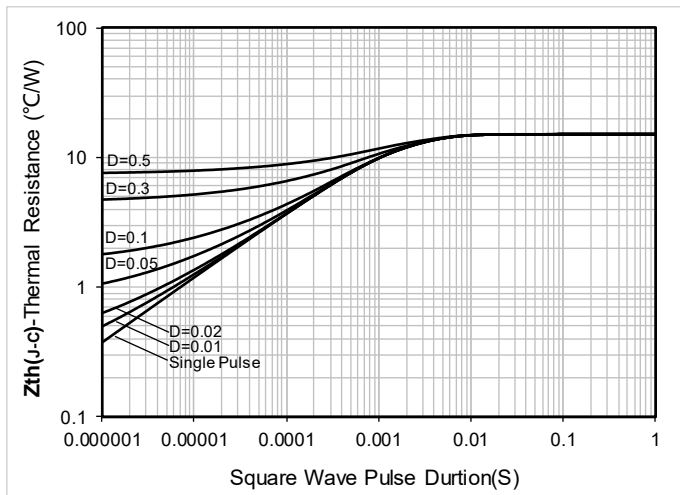


Figure 13. Maximum Transient Thermal Impedance

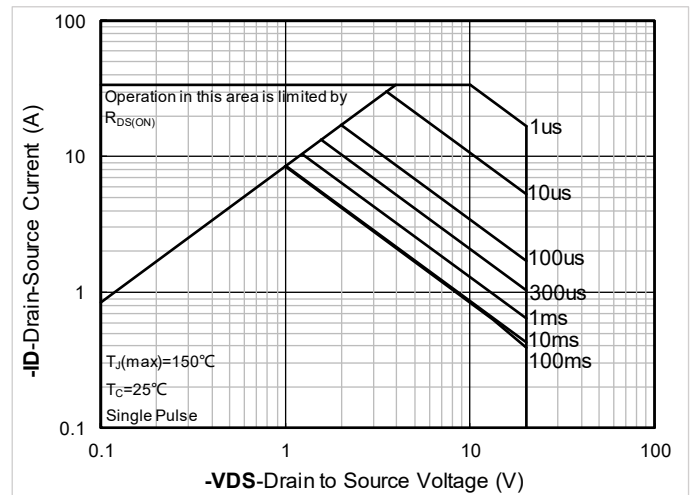
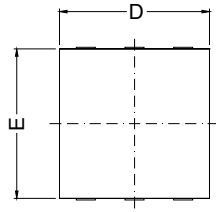


Figure 14. Safe Operation Area

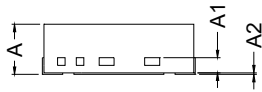


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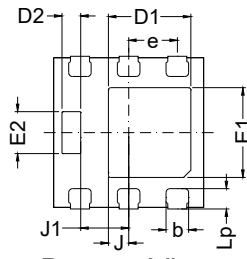
■ DFN2020-6L-H-0.65MM Package information



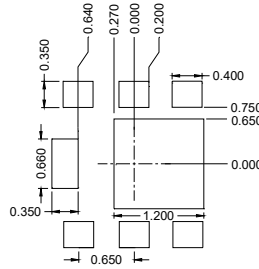
Top View
正面视图



Side View
侧面视图



Bottom View
背面视图



Suggested Solder Pad Layout
Top View

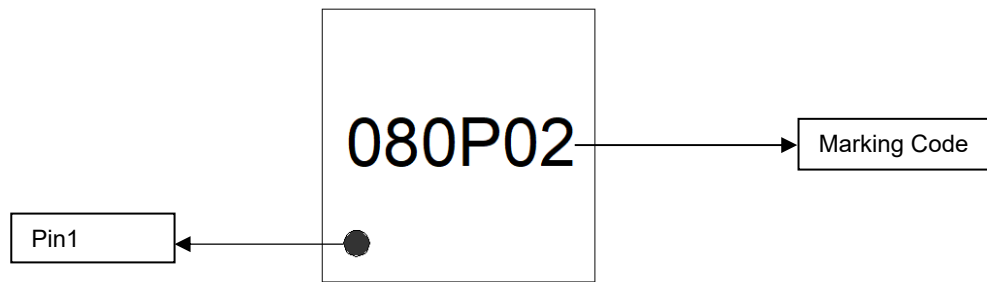
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	1.90	2.00	2.10
E	1.90	2.00	2.10
A	0.55	0.65	0.75
A1	0.20 BSC		
A2	0	-	0.10
D1	1.00	1.10	1.20
D2	0.20	0.25	0.35
E1	1.10	1.20	1.30
E2	0.51	0.56	0.66
Lp	0.20	0.25	0.35
J	0.27 BSC		
J1	0.64 BSC		
b	0.20	0.30	0.40
e	0.65 BSC		

Note:

1. Controlling dimension: in millimeters.
2. General tolerance: ± 0.10 mm.
3. The pad layout is for reference purposes only.



■ Marking Information



- Note:
1. All marking is at middle of the product body
 2. All marking is in laser printing
 3. 080P02 is marking code
 4. Body color: Black



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